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10/705,843	11/13/2003	Alexander Krymski	M4065.0960/P960	4875

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EXAMINER	
LUU, THANH X	

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 05/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/705,843	KRYMSKI, ALEXANDER	
	Examiner	Art Unit	
	Thanh X. Luu	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-20,22-31 and 33-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-20,22-31 and 33-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 13, 2006 has been entered.

Claims 1, 3-20, 22-31 and 33-36 are currently pending.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 3, 26, 28 and 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 is dependent from a cancelled claim.

Regarding claim 26, "said stored signals" and "said readout circuits" lack proper antecedent basis.

Regarding claim 28, "respective ones of a plurality of capacitive elements" lacks proper antecedent basis. Furthermore, it is unclear how the capacitive elements are related to the charge storage devices.

Regarding claim 30, "each respective readout circuit" lacks proper antecedent

basis.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 20, 26-29 and 31, as understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Pain et al. (WO 99/482281).

Regarding claims 20 and 31, Pain et al. disclose (see Figs. 1, 2 and page 6, lines 17-30) a charge-domain readout circuit, comprising: a plurality of column readout circuits each of which sample and combine multiple pixel signals and reset signal values of a plurality of pixels of an active pixel sensor, wherein each column readout circuit is associated with a respective column of sensors in the active pixel sensor, each column readout circuit comprising: a plurality of charge storage devices (CIS, CIR) for respectively (CIS stores pixel signals; CIR stores reset signals) storing each of the multiple pixel signals and reset signal values, and a combining circuit (various switches) for combining the respectively stored multiple pixel signals and reset signal values; a first bus (output line) for receiving pixel signal values stored by a selected one of the column readout circuits; and a second bus (another output line) for receiving the reset

signal values stored by a selected one of the column readout circuits. A processing circuit is inherent in the image sensing system of Pain et al.

Regarding claims 26-29, Pain et al. disclose (see Figs. 1, 2 and page 6, lines 17-30) a method of reading out values from active pixels sensors in an array of sensors, comprising: selective multiple rows of sensors whose values are to be read out; storing (with CIS and CIR) correlated double sampled values for a plurality of sensors in the selected rows, wherein the values for each sensor are stored by a respective pair of charge storage devices (CIS and CIR) in a readout circuit associated with a column in the array in which the sensor is located; combining (with the various switches) the stored values and sensing the stored values using an operational amplifier-based charge sensing circuit (A or AO) as claimed. Pain et al. also disclose (see Fig. 2) setting a reference voltage (V+) on first sides of respective capacitive elements (CLS, CLR) as claimed.

6. Claims 1, 3-13, 18, 20, 22, 24, 31 and 33, as understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Yang et al. (U.S. Patent Application Publication 2004/0246354).

Regarding claims 1 and 3-5, Yang et al. disclose (see Fig. 2) an image sensor readout circuit, comprising: a column line (col 1 and col 2) for receiving a plurality of analog pixel (light) and analog reset (reference) signals; and a binning circuit (303) coupled to the column line, wherein the binning circuit comprises: a first plurality of charge storage devices (CAP C1, CAP C2) for respectively storing a predetermined plurality of analog pixel signals from a plurality of pixels, a first combining circuit (S1 top,

C1, C2) for combining the stored plurality of analog pixel signals and outputting them on a first output line, a second plurality of charge storage devices (CAP R1, CAP R2) for respectively storing a predetermined plurality of analog reset signals from a plurality of pixels and a second combining circuit (S1 bottom) for combining the stored plurality of analog reset signals and outputting them on a second output line. Yang et al. also disclose (see Fig. 2) the first combining circuit comprises a first plurality of sample switches (C1, C2), the first plurality of charge storage devices comprises a first plurality of capacitive elements and wherein each of the sample switches is coupled to one of the respective capacitive elements and the capacitive elements being further coupled to the first output line. Yang et al. further disclose (see Fig. 2) the second combining circuit comprises a second plurality of sample switches (R1, R2), the second plurality of charge storage devices comprises a second plurality of capacitive elements and wherein each of the sample switches is coupled to one of the respective capacitive elements and the capacitive elements being further coupled to the second output line. The number of sample switches and capacitive elements is even.

Regarding claims 6-9, Yang et al. disclose (see Fig. 2) a binning circuit for an image sensor, comprising: a column line (col 1 and col 2) for receiving analog pixel (light) and analog reset (reference) signals of an active pixel sensor; a first sample circuit (C1, C2, CAP C1, CAP C2) coupled to the column line, the first sample circuit comprising a first plurality of charge storage devices (CAP C1, CAP C2) respectively storing a plurality of analog pixel signals from a plurality of pixels; a second sample circuit (R1, R2, CAP R1, CAP R2) coupled to the column line, the second sample circuit

comprising a second plurality of charge storage devices (CAP R1, CAP R2) respectively storing a plurality of analog reset signals from a plurality of pixels; a first switch (S1 top) coupled to the first sample circuit and to a first output line to combine the stored pixel signals and output the combined pixel signals on the first output line; and a second switch (S1 bottom) coupled to the second sample circuit and to a second output line to combine the stored plurality of reset signals and output the combine reset signal on the second output line. Yang et al. also disclose (see Fig. 2) the first sample circuit comprises a first plurality of sample switches (C1, C2), the first plurality of charge storage devices comprises a first plurality of capacitive elements and wherein each of the sample switches is coupled to one of the respective capacitive elements and the capacitive elements being further coupled to the first output line. Yang et al. further disclose (see Fig. 2) the second sample circuit comprises a second plurality of sample switches (R1, R2), the second plurality of charge storage devices comprises a second plurality of capacitive elements and wherein each of the sample switches is coupled to one of the respective capacitive elements and the capacitive elements being further coupled to the second output line. The number of sample switches and capacitive elements is even.

Regarding claims 10-13 and 18, Yang et al. disclose (see Fig. 2) a method of binning an output of an active image sensor, comprising: sampling and respectively storing (C1, C2, CAP C1, CAP C2) analog output (light) signals form a plurality of pixels of the sensor according to a first predetermined sequence; sampling and respectively storing (R1, R2, CAP R1, CAP R2) analog reset (reference) signals from a plurality of

pixels of the sensor according to a second predetermined sequence; subsequently combining (with S1 top) and outputting all sampled and respectively stored analog output signals on a first line; and combining (with S1 bottom) and outputting all sampled and respectively stored analog reset signals on a second line. Yang et al. also disclose respective capacitive elements (CAP C1, CAP C2, CAP R1, CAP R2) as claimed. Since the entire pixel array is not read out, as understood, there is a less-than-full pixel resolution condition as claimed. Yang et al. also disclose (see Fig. 2) subtracting (with 301) the combined analog output signal from the combined analog reset signal.

Regarding claims 20, 22, 24, 25, 31 and 33, Yang et al. disclose (see Figs. 1 and 2) a charge-domain readout circuit, comprising: a plurality of column readout circuits each of which sample and combine multiple pixel signals and reset signal values of a plurality of pixels of an active pixel sensor, wherein each column readout circuit is associated with a respective column (col 1 and col 2) of sensors in the active pixel sensor, each column readout circuit comprising: a plurality of charge storage devices (CAP C1, CAP C2, CAP R1, CAP R2) for respectively storing each of the multiple pixel signals and reset signal values, and a combining circuit (S1 top, C1, C2; S1 bottom, R1, R2) for combining the respectively stored multiple pixel signals and reset signal values; a first bus (output line) for receiving pixel signal values stored by a selected one of the column readout circuits; and a second bus (another output line) for receiving the reset signal values stored by a selected one of the column readout circuits. Yang et al. further disclose (see Fig. 2) a plurality of first switches (C1, C2) as claimed; and a switch (S1 top) that can be selectively enabled to short together one side of each of the

plurality of charge storage elements (CAP C1, CAP C2); and (see Fig. 1) column switches (bottom-most S1) coupled between each column readout circuit as claimed. A processing circuit is inherent in the image sensor system of Yang et al.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 14-17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. in view of Funakoshi et al. (U.S. Patent Application Publication 2002/0154347).

Regarding claims 14-17 and 19, Yang et al. disclose the claimed invention as set forth above. Yang et al. do not specifically disclose interpolating or sampling identical colors or the sequences determined by a Bayer pattern. Funakoshi et al. teach (see Figs. 10-12) interpolating by sampling identical colors from different rows that is determined by a Bayer pattern. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide such interpolation as claimed in the method of Yang et al. in view of Funakoshi et al. to obtain more accurate color imaging as taught.

9. Claims 23, 26-30 and 34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. in view of Applicant's Admitted Prior Art (Fig. 3), hereinafter, AAPA.

Regarding claims 26 and 27, Yang et al. disclose (see Fig. 2) a method of reading out values from active pixels sensors in an array of sensors, comprising: selective multiple rows of sensors whose values are to be read out; storing (with CAP C1, CAP C2, CAP R1, CAP R2) correlated double sampled values for a plurality of sensors in the selected rows, wherein the values for each sensor are stored by a respective pair of charge storage devices in a readout circuit associated with a column in the array in which the sensor is located; combining (with S1) the stored values and sensing (with 301) the stored values as claimed. Yang et al. do not specifically disclose sensing with an operational amplifier. AAPA teaches (see Fig. 3) correlated double sampling with an operational amplifier (112). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use an operational amplifier as claimed in the method of Yang et al. in view of AAPA to obtain effective and efficient sensing as taught.

Regarding claims 23, 28-30 and 34-36, Yang et al. disclose the claimed invention as set forth above. Yang et al. also disclose a crowbar switch (S1). Yang et al. do not specifically disclose setting a reference voltage on a first side of a charge storage device as claimed. AAPA teaches (see Fig. 3) setting a reference voltage (VCL) to first side of a charge storage device to set initial conditions and to the operational amplifier (112) and capacitive feedback elements in the operational amplifier. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide such a reference voltage setting in the method and apparatus of Yang et al. in view of AAPA to obtain more accurate results.

Response to Arguments

10. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

11. Applicant's arguments filed with respect to claims 20, 26 and 31 have been fully considered but they are not persuasive.

As understood, the charge storage devices of Pain et al. still read on the language of "a plurality of charge storage devices for respectively storing each of said multiple pixels signals and reset signal values...." That is, the CIS and CIR capacitors respectively store multiple pixel or reset signal values.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh X. Luu whose telephone number is 571-272-2441. The examiner can normally be reached on M-F 6:00AM-3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on 571-272-2328. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Thanh X Luu
Primary Examiner
Art Unit 2878

05/2006